UltraCAD Design, Inc.

DESIGN NOTE

THE EFFECTS OF VIAS ON PCB TRACES

Background:

Through the years we have worked with many engineers who have had strong feelings about the presence of vias on critical traces (such as fast rise time clock lines). These feelings have ranged from (a) the effects of vias are so negligible that they may be used freely, to (b) their effects are so significant that vias may not be used at all. Depending on your view, these two extremes place quite different constraints on PCB designs!

It is clear from the history of all the boards that have ever been designed in the past that vias have little impact at lower frequencies and rise times. It is only recently, as device rise times and timing issues caused by faster clock speeds have become critical PCB design issues, that the concern over a via's effect on PCB "transmission lines" has become a topic of discussion.

The perceived negative effects of vias may fall into one of several categories:

1. Vias are inherently capacitive and change the characteristic impedance of the trace.

2. Vias cause a step-function change in trace impedance and therefore cause reflections.

3. When a trace moves from one layer to another, it becomes referenced to a different reference plane, therefore severely distorting the characteristic impedance of the trace.

4. A trace can move to opposite sides of an individual reference plane without significant effect, but if it moves to a layer where it is referenced to a different plane then the characteristics of the transmission line are severely distorted.

5. The effect of the first via is the greatest, but the effects of additional vias diminish as more vias are added to the trace.

Unfortunately, there have been few, if any, studies specifically designed to study the effects of vias while adequately controlling for other variables. This is, at least in part, due to the resources required: (a) the design of a test board, (b) its fabrication, and (c) the availability of a proper suite of test equipment and the researchers skilled in knowing how to use it.

Strategy:

In order to clarify some of these issues, a study was designed in order to isolate and measure individual effects that vias might have on traces. A test board was designed with 9 dual stripline traces on it, each of identical length, width, and thickness. There were four trace layers and three reference planes designed into the board. Some traces had no vias on them at all --- they were "pure" transmission lines. Others had one or more via "holes" along them, but the signal path did not go through the vias. Others passed through the via, but the signal path always

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referenced the same plane. Finally, others passed through the via in such a way that the stripline trace referenced a different reference plane. Each trace was terminated at each end with a high-performance RF 50Ω connector, providing access for the test equipment.

Each trace was evaluated with a time domain reflectometer, and signals were visually evaluated at both the input and output.

This study presents a model of industry cooperation for the common goal of increasing understanding. The board design and project coordination was donated by UltraCAD Design, Inc. (Bellevue, WA.) Eight boards were fabricated and donated by Dynamic Circuits, Inc. (Milpitas, CA.) The test equipment and measurement resources were provided by Professors Chi H. Chan and Yasuo Kuga at the University of Washington's Electrical Engineering Department. And the Washington Technology Center provided matching funding for equipment and resource availability. None of these partners had all the resources required to do the research on their own. Their mutual cooperation made this effort possible.

Procedure:

The design of the test board is shown in Figures 1 and 2. Traces on layers 2, 3, 6, and 7 are identical width (.008 inches), length (15 inches) and thickness (one ounce copper, approximately .0014 inch thick). They all are dual stripline traces and are as close as possible to identical. Target characteristic impedance is 50Ω. Layers 1, 4+5, and 8 are planes (4 and 5 are electrically connected as a single plane.) The three planes are isolated from each other except for the capacitors C1 through C4. This configuration simulates a normal board with separate power and ground planes, capacitively filtered at some arbitrary spot on the board. Via holes are represented by circles along the trace. They are precisely placed along a grid that divides the trace length into eight equal increments. The vias themselves are .028 diameter plated through holes, with .050 diameter pads and .075 diameter anti-pads on the planes.

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The number along each trace segment identifies the layer it is on. Each trace is terminated at each end by a 50Ω RF connector. The shell of the connector is connected to one of the three planes as indicated by the number adjacent to the connector.

Each trace, in turn, was connected to an HP 54120B Time Domain Reflectometer (TDR) at the left side of the board. The other end of the trace was terminated in a 50Ω load. The TDR provides an output that can reflect the impedance at any point along the trace. Two different boards were evaluated in this manner, and the results compared. In addition, a fast rise time pulse was applied to each trace and the signal at the opposite end was recorded with a high frequency storage scope.

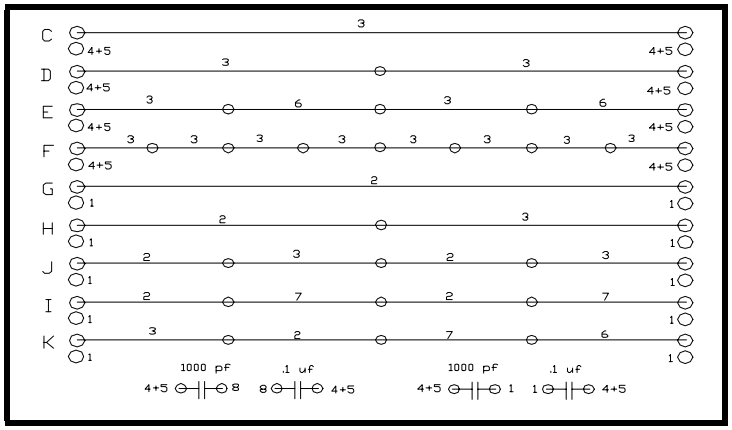


Figure 1
Board Schematic

Trace geometries are identical. Circles represent vias along the traces. The numbers on the trace segments or connector and component pins define the layers to which they are connected.

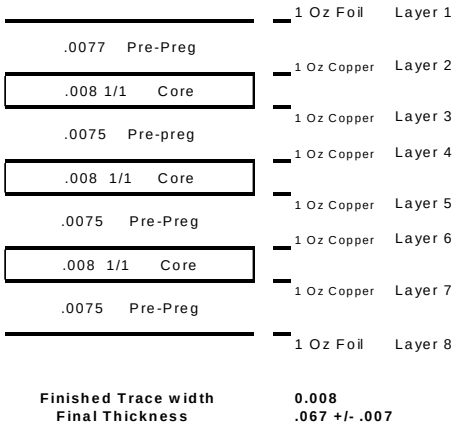
The traces reflect increasingly "worse" cases. Traces C and G (traces A and B applied to a different analysis) are pure transmission lines. Traces D and F have vias along them, but the signal does not pass through the vias. Other traces have vias through which the signal passes to various combinations of layers, involving one or more reference planes.

Results:

Figure 3 illustrates the TDR output for Trace C, a straight trace with no vias. It should be as close an approximation to a "pure" transmission line as can be achieved with this setup. The "round trip" time on the output is almost exactly 5 nsec. Although we do not favor using "rules of thumb", it is interesting to note that at 2 nsec per foot, the rule of thumb for pulse propagation delay along a trace, this equates exactly to the trace length of 15 inches!

The average measured impedance along the trace is about 58Ω, or about 16% over target. The variation in impedance along the trace ranges from 57.2Ω to 59.5Ω, or about 4% around the average.

Figure 4 illustrates the TDR outputs for Trace G for both board 1 and board 2, thus comparing the repeatability between boards. This trace is also a pure transmission line, but on trace layer 2. In theory, both traces should look the same



VIA Test Board
Layer Stack-up
(Not to Scale)

Figure 2

and they should look like the trace in Figure 3. In fact, while the average impedance for each trace is about 58Ω , the range of impedance is from 57 to 62Ω for board 1 and from 56 to 60Ω for board 2.

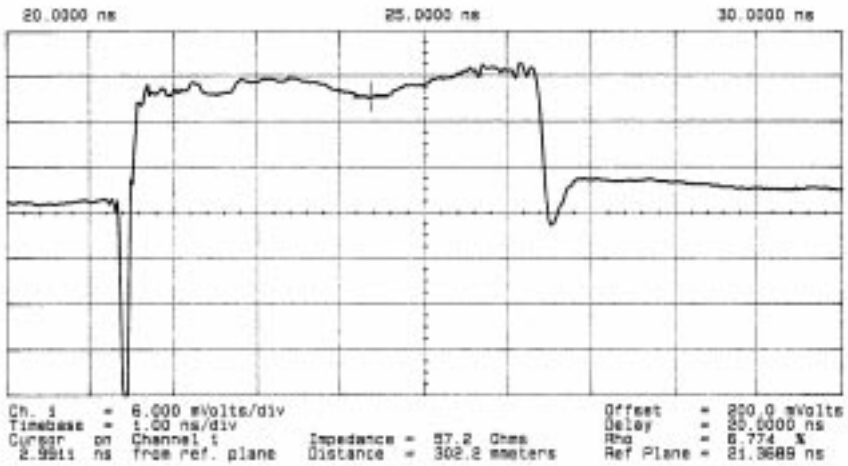
These figures illustrate the practical problem of specifying trace impedances on PCB boards. Even under reasonably controlled conditions, impedance targets are hard to hit, and they vary by several percent from board to board, from layer to layer, from trace to trace, and even along the same trace!

Figure 5 illustrates the TDR results for Trace D. This trace is on layer 3 with a single via in

Figure 3

TDR output for Trace C, Layer 3

The variation in impedance along the trace is approximately 2.3 Ω or about 4%. The "round trip" trace length is about 5 nsec, implying a 15" trace at a propagation delay of 2 nsec/ft.



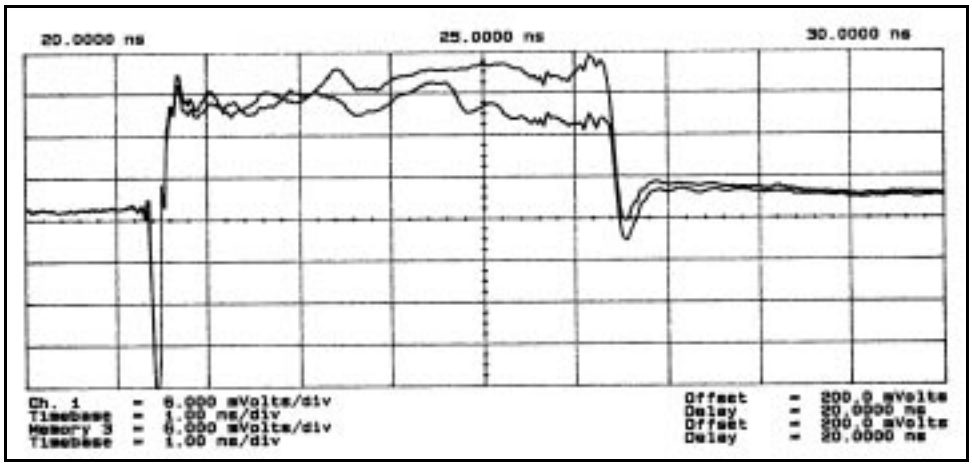


Figure 4

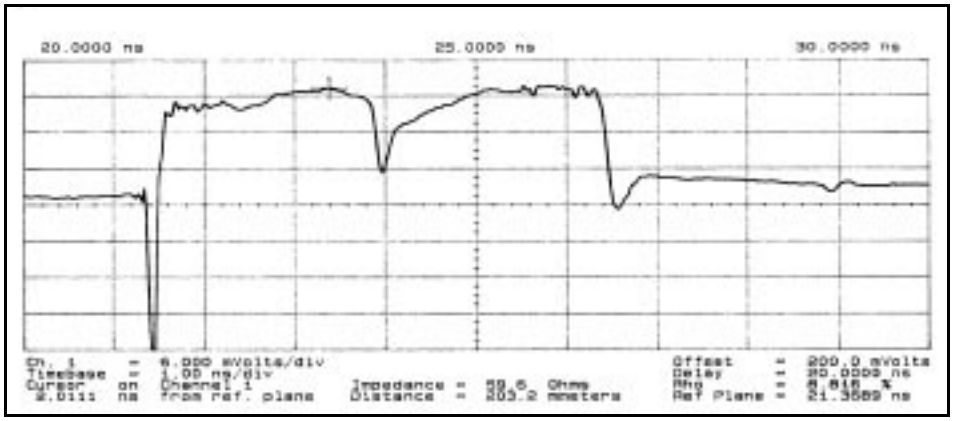
Comparative TDR outputs for Trace G, Boards 1 and 2, Layer 2.

Note the variation in impedance not only along the trace, but between the fabricated boards themselves.

Figure 5

Trace D, layer 3, with a single via in the center of the trace. The trace does not pass through the via.

Note that the region affected by the via is about +/-.5 in. Otherwise the trace closely resembles Figure 3 (Trace C).



the middle, but the signal does not pass through the via to another layer. Except for the via, the trace closely resembles Trace C (Figure 3), immediately adjacent to this trace and on the same layer. This result is typical; trace areas outside the influence of the vias exhibit very similar characteristics to adjacent traces on the same layer, but this similarity diminishes as the distance to adjacent traces increases.

The impact of the via suggests that the via is capacitive in nature, and the measured transient impedance drops about 6 or 7Ω (approximately 12%) at the lowest point.

The influence of the via is seen over about 300 Psec of trace length around the via, or almost +/-.5 inch, even though the maximum via geometry is only .075 inch. This result is consistent for all vias. This illustrates the degree that the transmission line assumptions break down in the region around the via. Although it was not studied in this effort, the region influenced by a component pin is presumably even larger.

Figure 6 illustrates what happens when more vias (7 of them) are added along the trace. Again, this trace is on layer 3 and the signal does not pass through any via. And again, the area between the vias resembles Trace C on layer 3 (with no vias) although this trace is somewhat further separated from Trace C.

The influence of the vias appears to decrease as more vias are added. We have heard engineers describe this effect as follows:

The first via has a significant capacitive effect, but this effect diminishes as more vias are added.

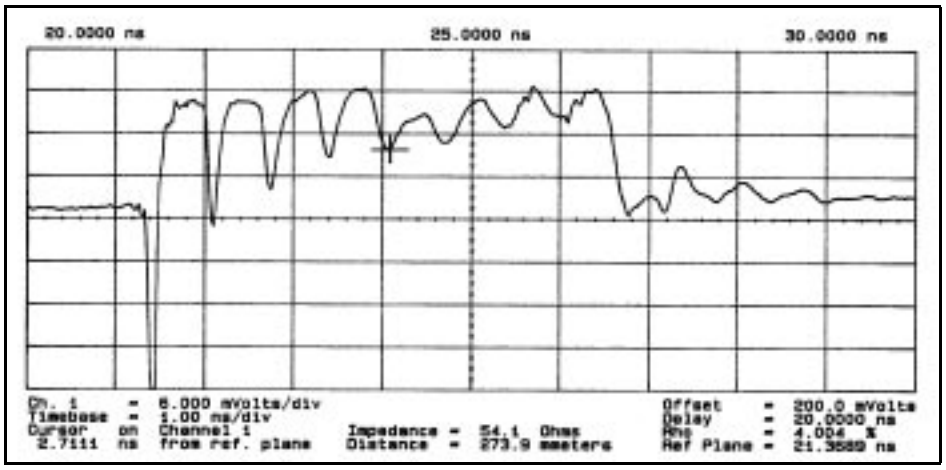
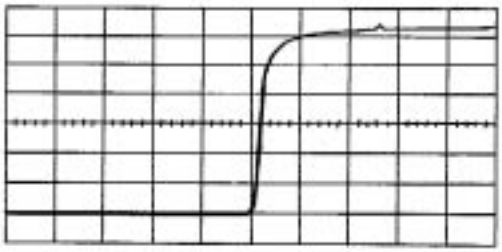


Figure 6, Trace F, layer 3 with multiple vias. Traces do not go through the vias.



Timebase = 1.00 ns/div
Ch. 4 = 50.00 mVolts/div

Figure 7

Trace D, Layer 3

Output from Trace in response to a step-function input. Rise time degredation is 191 Psec.

In fact, what appears to be happening is that each via (and even the trace itself) causes a slight high frequency loss (to be described in more detail, below.) This loss in high frequency component appears to manifest itself in measurement distortion within the TDR. Thus, the TDR appears to suggest decreasing effects as more vias are added because its own measurements are being distorted by the attenuation of higher frequency harmonics. This result is typical for all traces.

Another result tends to confirm this analysis. Figure 7 illustrates the output at the end of a typical trace as a result of a step-function input to the trace. (Figure 7 happens to illustrate Trace D.) The input voltage had a measured rise time of 40 Psec. The output signal from Trace C had a measured rise time of 231 Psec, or a slowing of the rise time by 191 Psec. This represents the attenuation of higher order frequency harmonics from trace losses (and perhaps connector losses) alone.

The measured rise time of Trace F (with 7 vias) was 376 Psec, suggesting the vias "cost" another 145 Psec in rise time, or about 20 Psecs per via. Other measurements along other traces were consistent with this estimate of 20 Psec reduction in rise time per via.

Interestingly enough, when the signal passed through a via to another layer, there were no additional effects that have not already been discussed. This was true even when the signal became referenced to a different plane. The effect in the immediate vicinity of the via hole was the same as if the signal did not pass through the via, and between the vias the traces took on the characteristics of layer they were on. There was some signal degradation due to the inherent nature of a transmission line and because of differences in impedance **along**

the trace. But using a via to transition to another layer of the same target impedance seemed to have no additional degradation than a did a via hole without a signal transition.

Conclusion:

In these results, a via tended to present a transient impedance discontinuity to a trace of about 6Ω. This would result in a negative reflection coefficient of about .055, or about 5%:

$$\rho = \frac{(R_L - Z_0)}{(R_L + Z_0)} = \frac{52 - 58}{52 + 58} = .055$$

Visual evaluation of various signals also suggested that reflections are small. (For example, see Figure 7.)

Vias did have a capacitive effect and tended to attenuate the very high frequency harmonics of the signal, as manifested in a slower signal rise time. But this effect, per via, was about an order of magnitude less than the losses along the trace without any vias at all (over the full 15 inches of trace). It would seem that for designs using components with rise times in the range of .5 to 1.0 nsec or slower (500 to 1000 Psecs), which is still pretty fast, a 40 Psec rise time impact as a result of a via would appear to be relatively harmless.

Other Considerations:

While the results of this study were consistent across traces and boards, they do raise some other questions. For example, would vias have relatively more impact if traces were shorter? Or if via geometries were larger? Or what if we targeted a different intrinsic impedance (such as 75Ω)? We think not, but the question deserves consideration.

If a via has an impact that is seen for as much as .5 inch around the via, how do component pins (as differentiated from the components themselves) impact trace impedances in dense boards?

Although there did not seem to be any signal degradation when a signal passed through a via and became referenced to a different plane (as in the case of Trace J where the trace is alternately referenced to the top plane -- layer 1-- and the middle plane -- layers 4+5), it nevertheless seems true that the signal return path must be somewhere. And other studies have shown that for fast rise time pulses, the **return** path likes to be "close" to the signal path. If the return paths are "roaming" unpredictably around the planes, does this have an impact for EMI radiation from the board? The answer might quite likely be "yes."

Thus, the results disclosed by this study seem to be instructive, but, as always, more questions are raised.